

**FIG.1**

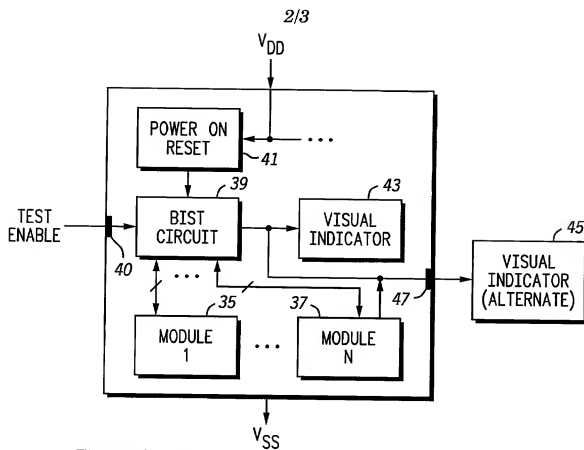


FIG. 2

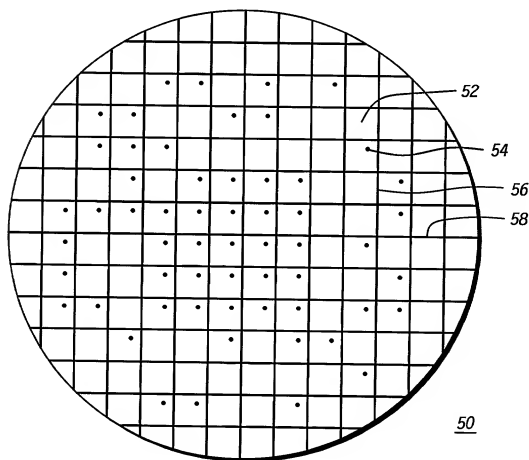
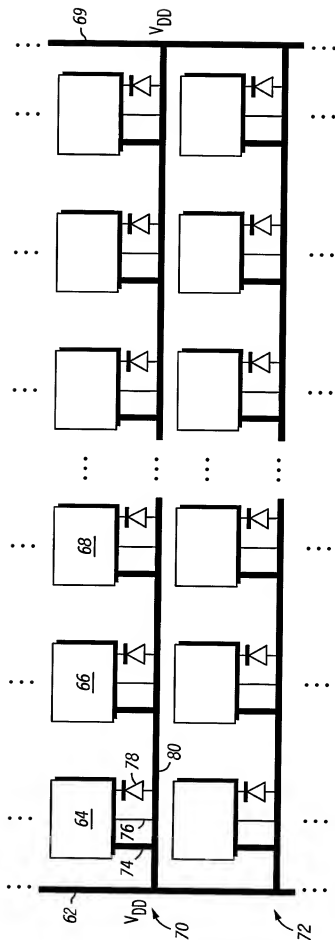


FIG. 3

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*FIG. 4*

FIG. 4 is a schematic diagram of a memory array structure. The array is composed of a plurality of memory cells (64, 66, 68) arranged in rows and columns. Each memory cell is connected to a word line (62, 69) and a bit line (70, 72). Access transistors (74, 76, 78) are used to connect the memory cells to the bit lines. The word lines and bit lines are connected to a supply voltage  $V_{DD}$ .